[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 4307 **G**

Unique Paper Code : 32341102

Name of the Paper : Computer System Architecture

Name of the Course : **B.Sc. (H) Computer Science**

Semester : I

Duration : 3 Hours Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. **Section A is compulsory.**
3. Attempt any four questions from **Section B**. Parts of a question must be answered together.

Section A

1. (a) Derive an algebraic expression for the complement **F'** of the given Boolean expression:

F=xy'z'+xy'. (2)

(b) Give any two differences between combinational and sequential circuit. (2)

(c) Determine the number of clock cycles that it takes to process 90 tasks in five segment pipeline. (2)

(d) What is flip flop? Give the truth table of SR flip flop. What is the drawback of SR flip flop? (3)

(e) Perform the following arithmetic operation:

(-19) + (-38)

(Use signed 2's complement representation for negative numbers and 8 bits to accommodate each number together with its sign.) (4)

(f) What is hardwired control unit? Give one advantage and one disadvantage of the same. (3)

(g) Draw instruction format for a 16-bit instruction that has 2048 words memory, 3 bits for opcode, and four addressing modes. (3)

(h) Write two instructions needed in the basic computer to set the extended bit **E** to 1. (2)

(i) Give one advantage and one disadvantage of isolated I/O. (2)

(j) Simplify the following Boolean function using a three variable Karnaugh map:

$F(x, y, z) = \Sigma(0, 2, 4, 5, 6)$.

Further, draw its simplified logic diagram. (4)

(k) Write the sequence of micro-operations for implementing **BSA** and **ISZ** instructions. (4)

(l) Draw the logic diagram and truth table of a **2x4** decoder using only **NAND** gates with enable input. (4)

Section B

2. (a) A computer uses a memory unit with 4096 words of 16 bits each. An instruction at address 03B in the basic computer has I=1, an operation code of the **ADD** (opcode 001) instruction, and an

address part equal to 075. The memory word at address 075 contains the value 032A. The memory word at address 32A contains the value 9C37 and the content of AC is 54AC. (all numbers are in hexadecimal)

(i) Give block diagram of memory unit to give snapshot of the above representation.

(ii) Go over the instruction cycle and determine the contents in hexadecimal of following registers: PC, AR, DR, AC, and IR when an instruction at address 03B is executed. Give the answer in a table with a column for each register and a row for each timing signal. (6)

(b) The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?

(i) 53K x 16

(ii) 24M x 32 (4)

3. (a) Perform the following conversions:

(i) $(237456)_{10} = (\ ?\ )_6$

(ii) $(2112110)_3 = (\ ?\ )_{10}$

(iii) $(EF345)_{16} = (\ ?\ )$

(iv) $(14.0625)_{10} = (\ ?\ )_2$

(v) $(280)_9 = (\ ?\ )_{10}$ (5)

(b) A non-pipeline system takes 30 ns to process a task. The same task can be processed in a four-segment pipeline with a clock cycle of 10 ns.

(i) Determine the speedup ratio of the pipeline for 100 tasks.

(ii) What is the maximum speed that can be achieved?

P.T.O.

(iii) Draw a space time diagram of the abo pipeline system for 8 tasks. (

4. (a) Write a program using one address and thre address instructions to evaluate the arithmeti expression:

$$X = (A-B) * (C + D)$$

Assume that memory operands are in memory addresses A, B, C and D and the result must be stored in memory at address X. (6)

(b) Construct a 4-to-16-line decoder using two 3 X 8 decoders with enable input. Give block diagram and function table of the same. (4)

5. (a) **Given F (A, B, C, D) = Σ (0, 2, 8, 9, 10, 11, 14, 15)**

(i) Simplify the function in product-of-sums form by means of a four-variable map.

(ii) Draw the logic diagram using OR-AND gates.

(iii) Specify the Boolean expression of the function without circuit simplification.

(iv) Compare the number of gates that would be required without circuit simplification against number of gates required with circuit simplification. (6)

(b) Represent the number $(+52.25)_{10}$ as a floating-point binary number with 24 bits. The normalized fraction mantissa has 16 bits, and the exponent has 8 bits. (4)

6. (a) Give block diagram of a Direct Memory Access (DMA) controller. How does CPU initialize the DMA transfer? (6)

(b) Write short notes on any two of the following:

(i) CPU Registers

(ii) Direct and Indirect Addressing Mode

(iii) Interrupt Cycle (4)